What is claimed is:

1. A semiconductor memory device having a bank for storing a data and a port as a data I/O terminal, comprising:

a global data bus for flowing an appearing current corresponding to the a data;

a plurality of first transceivers, in response to the inputted instruction, for delivering the data between a bank to the global data bus;

a plurality of first switching blocks, each for selectively connecting the global data bus to each of the plurality of first transceivers;

a plurality of second transceivers, in response to the inputted instruction, for delivering the data between a port and the global data bus; and

a plurality of second switching blocks, each for selectively connecting the global data bus to each of the plurality of the second transceivers,

wherein a swing range of a data bus voltage in response to the appearing current is narrower than a gap between a supply voltage and a ground.

2. The semiconductor memory device as recited in claim 1, wherein each of the first and second transceivers includes:

a transmitter, having a pull-down driver controlled by a control signal, for delivering the data inputted from the port or retrieved from the bank; and

a receiver for sensing the appearing current by using a current-mirror and delivering the data corresponding to the sensed appearing current into one of the bank and the port.

3. The semiconductor memory device as recited in claim 2, wherein the receiver includes:

a current mirror block for mirroring the current in the global data bus to output the current as the data; and

a latch block for latching the data outputted from the current mirror block.

4. The semiconductor memory device as recited in claim 3, wherein the current mirror block includes:

a current mirror for mirroring the current;

a current control block coupled between the current mirror and the global data bus for controlling amount of the current; and

a third switching block coupled to the current control block for enabling the output of the current mirror in response to a data control signal.

5. The semiconductor memory device as recited in claim 4, wherein the latch block includes:

an inverting block controlled by a data enable signal for inverting the data outputted from the current mirror block; and

a latch for latching the data.

6. The semiconductor memory device as recited in claim 5, wherein the current mirror includes:

a first PMOS transistor having a gate, a drain and a source, the gate and drain diode-connected, the source connected to a supply voltage; and

a second PMOS transistor having a gate, a drain and a source, the drain connected to an output node, the source connected to a supply voltage, the gate connected to the gate of the first PMOS transistor.

7. The semiconductor memory device as recited in claim 6, wherein the current control block includes:

a first NMOS transistor having a gate, a drain and a source, the gate coupled to a reference voltage, the source connected to the drain of the first PMOS transistor and the drain connected to the global data bus; and

a second NMOS transistor having a gate, a drain and a source, the gate coupled to the reference voltage, the source connected to the drain of the second PMOS.

8. The semiconductor memory device as recited in claim 7, wherein the third switching block includes

a third NMOS transistor having a gate, a drain and a source, the gate coupled to a data enable signal, the source connected to the drain of the second NMOS transistor and the drain connected to a ground.

9. The semiconductor memory device as recited in claim 5, wherein the inverting block includes:

a first PMOS transistor having a gate, a drain and a source, the gate coupled to the inverse data enable signal, the source connected to the supply voltage;

a second PMOS transistor having a gate, a drain and a source, the gate coupled to the first or second data outputted from the mirroring block, the source connected to the drain of the first PMOS transistor, the drain coupled to the latch;

a first NMOS transistor having a gate, a drain and a source, the gate coupled to the data enable signal, the drain connected to a ground; and

a second NMOS transistor having a gate, a drain and a source, the gate coupled to the first or second data outputted from the mirroring block, the drain connected to the source of the first NMOS transistor, the source coupled to the latch.

10. The semiconductor memory device as recited in claim 5, wherein the latch includes two inverters.

11. The semiconductor memory device as recited in claim 2, wherein the pull-down driver includes a NMOS transistor, coupled between the global data bus and a ground, having a gate coupled to the data.

12. The semiconductor memory device as recited in claim 1, wherein the first switching block includes a MOS transistor

having a gate, a drain and a source, the gate coupled to a second control signal in response to a column command related to the bank, each of the drain and the source connected to each of the first transceivers and the global data bus.

13. The semiconductor memory device as recited in claim 1, wherein the second switching block includes a MOS transistor having a gate, a drain and a source, the gate coupled to a second control signal in response to a column command related to the port, each of the drain and the source connected to each of the second transceivers and the global data bus.